IN THE TITLE

Please amend the title as follows:

SYSTEMS FOR PERFORMING TRAFFIC MANAGEMENT INCORPORATING SHAPING TECHNIQUES

IN THE SPECIFICATION

Please amend the specification as follows:

The paragraph beginning on page 4, line 1 is amended as follows:

In addition, to schedule wheel 124, the scheduler 108 may also identify 122 flows meriting best-effort service ("unshaped" traffic). The shaper ~~112~~ 110 can opportunistically service these best-effort flows using residual bandwidth left unscheduled by the schedule wheel 124.

The paragraph beginning on page 10, line 6 is amended as follows:

The vector 150 shown in FIG. 3 includes different hierarchical layers 150a, 150b, and 150c. The lowest layer 150c includes a bit identifying the occupancy of port "a" class "1 " entries for 32 slots. For example, bit-1 of lower layer 150 corresponds to the occupancy of a class "1" entry for port "a" in slot 1 of the schedule wheel. In the illustration, bit 152 (filled) identifies that the entry for class "1" for port "a" in slot 124a holds a virtual circuit candidate for transmission. Though FIG. 4 3 shows one set 150c of lower layer bits, the vector 150 actually includes n-sets. For example, 1024-sets of 32 bits would provide 1 bit for the 32K different slots of a schedule wheel.

The paragraph beginning on page 10, line 15 is amended as follows:

The middle layer 150b of the vector 150 includes bits identifying the aggregated occupancy of the lower layer sets 150c. For example, bit 154 of vector 150b identifies whether all of the 32-bits within lower layer set 150c are occupied. That is, bit 154 indicates whether any of the lower layer bits in set 150c are available. Since, not all of the bits of lower layer set 150c are occupied, the bit 154 is illustrated as blank (e.g., "off"). Again, while FIG. 4 3 shows only

one set of middle layer bits 150b, the vector 150 may include many different sets (e.g., 32-sets of 32 bits).

The paragraph beginning on page 11, line 1 is amended as follows:

The top layer 150a in FIG. 4 3 includes bits identifying occupancy of sets of the middle layer 150b bits. For example, as shown in FIG. 4, bit 156 of the top layer identifies whether all of the bits in the set 150b of middle layer bits are occupied. Thus, the bit identifies whether any of 32 bits in middle layer 150b are filled and, in turn, indicates whether any of 1024 bits in the lower layer are currently occupied.

The paragraph beginning on page 13, line 15 is amended as follows:

As shown, the network processor 200 features an interface 202 (e.g., an Internet eXchange bus interface) that can carries packets between the processor 200 and network components. For example, the bus may carry packets received via physical layer (PHY) components (e.g., wireless, optic, or copper PHYs) and link layer component(s) ~~222~~ (e.g., MACs and framers). The processor 200 also includes an interface 208 for communicating, for example, with a host. Such an interface may be a Peripheral Component Interconnect (PCI) type interface such as a PCI-X bus interface. The processor 200 also includes other components such as memory controllers 206, 212, a hash engine, and scratch pad memory.

The paragraph beginning on page 17, line 13 is amended as follows:

FIG. 7 illustrates yet another implementation. As shown, the scheduler process 108 is divided into threads on three different engines 108a, 108b, 108c. Scheduler threads in the first engine 108a handles best-effort traffic (much like engine 108a~~b~~ in FIG. 6), scheduler threads in

the second engine 108a handle VBR circuits; while scheduler threads in the third engine handle CBR circuits.